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EXAMINER	
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ART UNIT	PAPER NUMBER
1753	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/826,036	Applicant(s) Chapple-Sokol et al.
	Examiner Rodney McDonald	Art Unit 1753

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Feb 24, 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 4-8, 10, and 15-27* is/are pending in the application.

4a) Of the above, claim(s) ______ is/are withdrawn from consideration.

5)☐ Claim(s) ______ is/are allowed.

6)☒ Claim(s) *1, 2, 4-8, 10, and 15-27* is/are rejected.

7)☐ Claim(s) ______ is/are objected to.

8)☐ Claims ______ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ______ is/are a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on ______ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some* c)☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ______.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). ______

4) ☐ Interview Summary (PTO-413) Paper No(s). ______

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. This application contains claims 16-20 drawn to an invention nonelected with traverse in Paper No. 8. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP. § 821.01.

Claim Rejections - 35 USC § 112

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 is indefinite because it depends from a canceled claim. It is suggested to correct the dependency of this claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4-8, 10, 15 and 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desai et al. (U.S. Pat. 6,303,480) in view of Park (U.S. Pat. 6,281,118).

Desai et al. teach a method of forming an electrically conductive plug in an opening in a ***dielectric layer*** (i.e. sidewall material such as silicon dioxide see example below) of a substrate. (See Abstract) Fig. 1 shows a conventional semiconductor workpiece or substrate 10. The substrate is typically ***a silicon wafer***. (Column 2 lines 5-15) The substrate includes one or more regions 12 of semiconductor material or conductor material. A dielectric layer 14 is patterned with a number of ***openings 16*** so that each opening exposes an area of one of the semiconductor or metal regions 12, this area being termed the "contact area" or "exposed area" of the semiconductor or metal region. (Column 2 lines 16-22)

As shown in FIG. 3, each opening 16 is filled with a metal or other conductive material 20 to form a "plug" that makes electrical contact with the underlying semiconductor or metal region 12. The plug also is called either a "contact" or a "via" according to whether the underlying region 12 is a semiconductor region or a metal interconnect, respectively. (Column 2 lines 28-34)

When the region 12 underlying the plug 20 is a semiconductor material, often a contact layer 22 is deposited directly over the semiconductor region. The contact layer is composed of a metal whose atoms do not substantially diffuse into the semiconductor 12, but into which a small amount of the semiconductor material diffuses to form a good electrical contact. For example, when the underlying region 12 is silicon, ***a titanium contact layer 22*** typically is deposited over the silicon. ***Subsequent annealing*** causes silicon to diffuse into the titanium to form ***titanium silicide***. (Column 2 lines 35-44)

A diffusion barrier layer 24 (i.e. liner) typically is deposited over the contact layer before depositing the plug material 20. ***The barrier layer 24*** (i.e. liner) prevents metal atoms of the plug material from diffusing into and contaminating the semiconductor 12. ***The most commonly used material for the diffusion barrier is titanium nitride.*** (Column 2 lines 45-50)

To minimize agglomeration of the plug material 20 while it is being deposited in the opening, the side wall of each opening typically is covered with ***a wetting or adhesion layer 26*** composed of a material having high adhesion to the plug material. When the plug material is tungsten or aluminum, typical materials used for ***the wetting/adhesion layer are titanium or a compound of titanium such as titanium nitride,*** titanium tungsten, or titanium silicide. (Column 2 lines 51-58)

Because titanium nitride has both barrier properties and wetting properties, ***a single layer of titanium nitride can be deposited to function as both the barrier layer 24 and the wetting layer 26.*** (Column 2 lines 59-62)

Finally, ***the remainder of the opening is filled with a conductive material 20, such as tungsten*** or aluminum, to form the plug. (Column 2 lines 63-65)

Each layer 20-26 typically is deposited either by a sputter deposition process or by a chemical vapor deposition process. (Column 3 lines 1-3)

We discovered that such openings could be successfully filled without voids by depositing ***a layer of silicon 30 over the titanium nitride barrier layer 24 and wetting/adhesion layer 26*** (i.e. "and" indicates a Si layer over both layers) as shown in FIG. 2, and ***then filling the opening***

with conductive material 20 by conventional CVD. We discovered that the silicon layer promotes the formation of a continuous nucleation layer rather than discrete "islands" of isolated nucleation sites during initial deposition of the conductive material, which results in the deposition of a continuous, smooth, homogeneous layer of the conductive material that appears to have very few grain boundaries. (Column 3 lines 48-52)

The chemical vapor deposition process used to deposit the metal or other conductive material 20 over the silicon layer 30 can be any CVD process that includes a precursor gas that can react with the silicon layer 30 to deposit the conductive material onto the walls of the openings 16. (i.e. sacrificial silicon layer) (Column 4 lines 6-11)

Our preferred process for depositing the silicon deposits *a layer of silicon 30 that is only one atomic layer deep.* (Column 4 lines 28-30)

We expect depositing a silicon layer 3 before performing chemical vapor deposition of the conductive material 20 to fill the opening will improve the homogeneity of the conductive material so as to prevent the formation of voids in the plug and reduce the number of grain boundaries in the material. (Column 4 lines 61-68)

To simulate a surface chemistry identical to that which typically would be found on the bottom or side wall of a opening for a plug, we formed the following successive layers on a 200 mm silicon wafer: (1) We grew a 3000 Angstroms layer of *silicon oxide* (i.e. simulates sidewalls) by annealing the silicon wafer in an oxygen atmosphere at a wafer temperature of 1000 degrees C.; (2) We deposited 200 to 300 Angstroms of titanium by ionized metal plasma sputter

deposition; (3) We deposited 100 Angstroms of titanium nitride by an MOCVD process employing thermal decomposition of tetrakis (dimethylamide) titanium (IDMAT); (4) Some of the wafers then were exposed to a plasma to drive out the oxygen, carbon and other impurities from the titanium nitride and to densify the titanium nitride; (5) One some of the wafers we deposited a single atomic layer of silicon by thermal decomposition of silane, using the silicon deposition process described below; then (6) We deposited tungsten in a thermal CVD process performed at a chamber pressure of 30 Torr, with a gas mixture of the following gases and flow rates: WF6 at 30 sccm, SiH4 at 30 sccm, Ar at 2500 sccm, and H2 at 1000 sccm. (Column 5 lines 17-37)

The differences between Desai et al. and the present claims is that the temperature of the CVD process for depositing the conductive contact is not discussed, the silicon being a polysilicon film is not discussed and the temperature for CVD of the layers is not discussed.

Park teach in FIG. 2A, a first doped polysilicon layer 22a and a first tungsten silicide(WSix; x=2 to 2.8) layer 22b are sequentially formed on a semiconductor substrate 20. Here, the first doped polysilicon layer 22a is formed by Chemical Vapor Deposition(CVD) using SiH.sub.4 gas as reactive gas and using PH.sub.3 gas as dopant at the temperature of 500 to 700.degree. C. Preferably, the ratio of SiH.sub.4 :PH.sub.3 is 1.1:1.5 to .5:1.8 and the deposition thickness of the first doped polysilicon layer 22a is 500 to 1,500 .ANG.. The first tungsten silicide layer 22b is formed by CVD using SiH.sub.2 Cl.sub.2 gas and WF.sub.6 has at the temperature of 500 to 650.degree. C. Preferably, the ratio of SiH.sub.2 Cl.sub.2 :WF.sub.6

is 2:1 to 3:1.5 and the deposition thickness of the first tungsten silicide layer 22b is 500 to 1,500 .ANG. (Column 3 lines 5-17)

Thereafter, the first tungsten silicide layer 22b and the first doped polysilicon layer 22a are patterned to form a word line 22. An intermediate insulating layer 24 is then formed on the overall substrate and etched by an etching using plasma gas, to expose the portions of the surface of the first tungsten silicide layer 22b of the word line 22, thereby forming a contact hole 26. (Column 3 lines 18-25)

Thereafter, a second doped ***polysilicon layer*** 28a and a second ***tungsten*** silicide layer 28b are sequentially formed on the surface of the contact hole 26 and on the intermediate insulating layer 24 and patterned, to a bit line 28 being in contact with the word line 22, as shown in FIG. 2C. Here, the second doped polysilicon layer 28a and the second tungsten silicide layer are formed under the same condition as the first doped polysilicon layer 22a and the first tungsten silicide layer 22b. That is, ***the second doped polysilicon layer 28a is formed by CVD using SiH.sub.4 gas as reactive gas and using PH.sub.3 gas as dopant at the temperature of 500 to 700.degree. C.*** Preferably, the ratio of SiH.sub.4 :PH.sub.3 is 1.1:1.5 to 1.5:1.8 and the deposition thickness of the second doped polysilicon layer 22a is 500 to 1,500 .ANG.. ***The second tungsten silicide layer 28b is formed by CVD using SiH.sub.2 Cl.sub.2 gas and WF.sub.6 gas at the temperature of 500 to 650.degree. C.*** Preferably, the ratio of SiH.sub.2 Cl.sub.2 :WF.sub.6 is 2:1 to 3:1.5 and the deposition thickness of the second tungsten silicide layer 22b is 500 to 1,500 .ANG. (Column 3 lines 50-68)

The motivation for depositing a polysilicon is that it allows for stabilizing a contact interface. (Column 2 lines 18-20) The motivation for utilizing temperatures during CVD is that it allows for deposition of the layers. (Column 3 lines 50-68)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Desai et al. by utilizing polysilicon and certain deposition temperatures as taught by Park because it allows for stabilizing a contact interface and for the deposition of layers.

Response to Arguments

5. Applicant's arguments filed 2-24-03 have been fully considered but they are not persuasive.

RESPONSE TO ARGUMENTS:

The 35 U.S.C. 102 rejections have been overcome. The 35 U.S.C. 103 rejection remains.

In response to the argument that Desai fail to teach a sacrificial layer that is deposited at a temperature range of 500 to 650 degrees C, it is argued that Desai do teach depositing a sacrificial layer of silicon 30 that can react with metal depositing gas which forms volatile compounds that can be readily evacuated from the process chamber. (See Desai et al. Column 4 lines 6-16) As to the temperature range involved Park suggest the required temperature range for depositing silicon and Desai et al. do not limit their temperature to 425 degrees C. (See Desai et al. discussed above)

In response to the argument that Desai et al. do not teach the required temperature range, it is argued that Park was relied upon to teach the required temperature range. (See Park discussed above)

In response to the argument that Park fail to teach depositing W at a lower temperature than that of the silicon layer, it is argued that Park suggest temperature ranges where W can be deposited at a lower temperature than that of the silicon. (See Park discussed above)

In response to the argument that Park would not lead one of ordinary skill in the art to deposit W at a lower temperature range than the silicon layer, it is argued that Park do suggest temperature ranges which would allow the W layer to be deposited at a temperature lower than the silicon layer which Applicant's claims require. Furthermore Applicant's specification does not give reasons or significance as to why one of ordinary skill in the art would choose to deposit the W layer at a temperature lower than the silicon layer. Therefore selecting a range with a known range as is taught by Park is obvious. (See Park discussed above)

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney McDonald whose telephone number is 703-308-3807. The examiner can normally be reached on M-Th from 8 to 5:30. The examiner can also be reached on alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen, can be reached on (703) 308-3322. The fax phone number for the organization where this application or proceeding is assigned is 703-873-9310.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

RODNEY G. MCDONALD
PRIMARY EXAMINER

RM

May 12, 2003